REMARKS

Claims 1-21 were pending in the application. In response to the Office Action, applicants have amended the drawings and the specification, canceled claims 1-21 and added new claims 22-39. Claims 22-39 are now pending for reconsideration.

Claims 1-21 are cancelled and claims 22-39 are added for business reasons not related to patentability or the cited references. Applicants disagree with and do not acquiesce to the rejection of claims 1-21. For business reasons not related to patentability, in particular to address a business need of the applicants, applicants have decided to present a different set of claims for prosecution in the present application. Applicants reserve the right to pursue the cancelled claims or other claims in one or more continuation applications.

The drawings were objected because of various editorial errors and informalities. Applicants have submitted herewith a set of proposed drawings changes and formal drawings incorporating the changes to address both the Examiner's and the Draftperson's objections.

The specification was objected to because of various informalities. The specification has been amended to correct the noted objection as well as other editorial errors. No new matter has been added.

Claims 1-21 were objected to because of a non-preferred dependency structure. Claims 18 and 20 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-2, 7-9, 14-16, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Selvidge et al. (U.S. Patent 5,649,176). Claims 3-6, 10-13, and 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Selvidge in view of Knapp et al (U.S. Patent No. 6,370,493). Applicants have canceled claims 1-21, rendering these rejections moot.

Applicants submit that the newly added claims 22-39 are patentable over the cited references. By way of background, the invention as presently claimed is directed to the problem of test pattern generation for a circuit which may have a race condition which requires race resolution in order to generate a valid test pattern. Neither of the cited references are directed to this problem.

The Office Action admits that Selvidge is not directed to test pattern generation and relies on Knapp for this missing teaching. However, Selvidge is directed to the problem of configuring Field Programmable Gate Arrays (FPGAs) and Knapp is only generally directed to test pattern generation and is more particularly directed to the problem of reducing iteration times for a simulation by querying the user to identify which pins in a model have changed. Neither of these references even mentions the problem of race resolution for test pattern generation.

Assuming for the sake of argument that there is any motivation to combine these references, the resulting combination would at best be a system for configuring FPGAs that reduces iteration time by querying the user to identify which pins of the FPGA model have changed. Applicants submit that absent the teachings of the present application there is no motivation to combine the cited references in a manner which bears on the patentability of claims 22-39.

In view of the foregoing, favorable reconsideration is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

October 17, 2003
Date

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